

Claims:

1. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:
 - a) depositing a generally conformal first barrier layer in the hole;
 - b) removing the first barrier layer formed on the bottom of the hole;
 - c) sputter depositing a second barrier layer under conditions of a high density plasma;and
 - d) depositing a metal layer in the hole.
2. The method of claim 1 wherein the first barrier layer is deposited using chemical vapor deposition techniques.
3. The method of claim 2 wherein the barrier layer is comprised of Si_xN_y .
4. The method of claim 3 wherein a portion of the first barrier layer formed on the bottom of the hole is removed using etching techniques.
5. The method of claim 4 wherein the metal layer deposited in the hole is copper.
6. The method of claim 5 wherein the metal layer is deposited using chemical vapor deposition techniques.
7. The method of claim 5 wherein the metal layer is deposited using physical vapor deposition techniques.
8. The method of claim 1 wherein the first barrier layer comprises Si_xN_y .

2 9. The method of claim 8 wherein the second barrier layer comprises a material selected from
3 the group consisting of Ta, TaN, TaSiN, TiSiN and combinations thereof.

1 10. The method of claim 9 wherein the metal layer sputter deposited in the hole is copper.

1 11. The method of claim 10 wherein the second barrier layer is sputter deposited under the
2 conditions of a high density plasma.

1 12. The method of claim 11 wherein the metal is sputter deposited under the conditions of a high
2 density plasma.

1 13. The method of claim 12 wherein the metal is heated to a temperature of between about room
2 temperature and about 500°C and then subjected to a pressurized environment.

1 14. The method of claim 13 wherein the pressurized environment is in the range of about 1000
2 psi to about 100,000 psi.

1 15. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:
2 a) depositing a first barrier layer over a blanket dielectric layer;
3 b) forming a hole through the barrier layer and the dielectric layer to expose an
4 underlayer;
5 c) depositing a second generally conformal barrier layer in the hole;
6 d) removing the barrier layer formed at the bottom of the hole;
7 e) selectively depositing a metal layer in the hole.

1 16. The method of claim 15 wherein the first barrier and second barrier layers are comprised of

2 Si_xN_y .

1 17. The method of claim 16 wherein the first and second barrier layers are formed using chemical
2 vapor deposition techniques.

1 18. The method of claim 17 wherein the barrier layer formed on the bottom of the hole is
2 removed by sputter etching techniques.

1 19. An integrated processing tool, comprising:
2 a central transfer chamber having a robot assembly disposed at least partially therein for
3 moving substrates;
4 a chemical vapor deposition chamber for depositing Si_xN_y ;
5 a high density plasma physical vapor deposition chamber connected to the transfer chamber
6 having a target comprising tantalum;
7 an etch chamber capable of achieving a high density plasma; and
8 a high density plasma physical vapor deposition chamber connected to the transfer chamber
9 having a target comprising copper.

1 20. The method of claim 5 wherein the metal layer is deposited by first depositing a wetting layer
2 using chemical vapor deposition techniques and then filling the hole using physical vapor deposition
3 techniques.

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